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EXAMINER	
PATEL, NIKETA I	
ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/528,474	TEE ET AL.	
	Examiner	Art Unit	
	NIKETA I. PATEL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amended Claims and Arguments/Remarks as field on 1/7/2008.

Response to Arguments

3. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. The indicated allowability of claim 2 is withdrawn in view of the newly discovered reference(s) to Leydier et al. No.: US 2004/0148539 A1. Rejections based on the newly cited reference(s) follow.

Drawings

5. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because numerical labels provided for the elements in figures 1, 2 and 3 are not sufficient. Each of the elements should be labeled with a text label such as ‘USB host controller’ for element 12 of figure 1. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

7. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The independent claims 1, 3, 5 and 6 recite various elements such as 'fist external terminals', ‘a USB bus’, ‘a USB interface’, ‘a host interface’, ‘a device interface' and 'second external terminals' however, the structural relations between these elements is missing. It is unclear as to how each of these elements function together to form various claimed embodiments. The dependent claims inherit the same deficiency.

b. Claim 1, recites ‘fist external terminal’ and ‘second external terminals’ and ‘third external terminals’, it is unclear how this limitations are implemented on "an interface integrated circuit" of claim 1. Are the terminals external to the interface integrated circuit?

c. Through out the claim language a use of acronym “USB” is used. Applicant must spell the acronym at least once at the first occurrence of the use.

d. Claim 2, lines 3-4 recites, ‘for connection to an external USB device controller **without and with** an external transceiver’. It is unclear to the examiner how the limitation of “without and with an external transceiver” can be implemented concurrently.

e. Applicant is kindly requested to thoroughly review the claim language as well as the specification and make appropriate corrections.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. As far as the examiner can interpret the claims in light of the 35 USC 112 rejection set forth above, claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication granted to Leydier et al. No.: US 2004/0148539 A1 (hereinafter “Leydier”.)

12. Referring to claim 1, Leydier teaches an interface integrated circuit device for interfacing a USB connection to a further circuit, the interface integrated circuit comprising: first external terminals for connecting to a USB bus [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; a transceiver capable of transceiving for both a USB host and a USB device, the transceiver having a USB interface, a host interface and a device interface, the USB interface being coupled to the first external terminals [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; second external terminals coupled to the device interface for connection to an external USB device controller [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; a host controller coupled to the host interface, the host controller having a parallel data/address bus [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; third external

terminals coupled to the parallel data/address bus [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

13. Referring to claim 2, Leydier teaches an integrated circuit device according to claim 1, wherein the device interface comprises both an analog USB device interface and a transceived digital USB device interface for connection to an external USB device controller without and with an external transceiver, respectively [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

14. Referring to claim 3, Leydier teaches an electronic apparatus with a USB connection, the electronic apparatus comprising: a functional circuit with a processor[figures 3, 4, 5 and paragraphs 52-58 and 63-69], a parallel address data bus coupled to the processor and a USB device controller circuit with a USB interface in parallel with said address/data bus, and an interface integrated circuit electronically between the USB connection on the one hand and the parallel address/data bus interface and the USB interface on the other hand[figures 3, 4, 5 and paragraphs 52-58 and 63-69], the interface integrated circuit including first external terminals for connecting to the USB connection[figures 3, 4, 5 and paragraphs 52-58 and 63-69]; a transceiver capable of transceiving for both a USB host and a USB device, the transceiver having a USB interface, a host interface and a device interface, the USB interface being coupled to the first external terminals[figures 3, 4, 5 and paragraphs 52-58 and 63-69]; the device interface being connected to the USB device controller circuit in said functional circuit [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; and a host controller coupled to the host interface, the host

controller being coupled to the processor via the parallel data/address bus [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

15. Referring to claim 4, Leydier teaches an electronic apparatus according to claim 3, wherein the apparatus is arranged to use USB communication from said host controller via the USB connection in a first speed mode when operating as USB host and to use USB communication via the USB connection in a second speed mode, different from said first speed mode, as determined by the device controller when operating as USB device [figures 3, 4, 5 and paragraphs 52-58 and 63-69].

16. Referring to claim 5, Leydier teaches an electronic system comprising a USB bus connection; a host apparatus and a device apparatus, at least one of the host and the device apparatus including a functional circuit with a processor, a parallel address data bus coupled to the processor and a USB device controller circuit with a USB interface in parallel with said address/data bus[figures 3, 4, 5 and paragraphs 52-58 and 63-69]: and an interface integrated circuit electronically between the USB bus connection on the one hand and the parallel address/data bus interface and the USB interface on the other hand, the interface integrated circuit including-first external terminals for connecting to a the USB bus connection [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; a transceiver capable of transceiving for both a USB host and a USB device, the transceiver having a USB interface, a host interface and a device interface, the USB interface being coupled to the first external terminals [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; the device interface being connected to the USB

device controller circuit [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; a host controller coupled to the host interface, the host controller being coupled to the processor via the parallel data/address bus [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

17. Referring to claim 6, Leydier teaches a method of operating an interface integrated in a USB system, the method comprising: receiving a selection whether the apparatus containing the interface integrated circuit should operate as a USB host or as a USB device [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; transceiving USB signals with a transceiver in the interface integrated circuit [figures 3, 4, 5 and paragraphs 52-58 and 63-69]; sequencing USB communication via the transceiver with a host controller in the interface integrated circuit and communicating USB transceived data to or from functional circuits outside the integrated circuit via a parallel address data interface when USB host operation is selected, and passing USB signals from the transceiver to a device controller in the functional circuits outside the integrated circuit when USB device controller operation is required [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

18. Referring to claim 7, Leydier teaches a method according to claim 6, wherein passing USB signals from the transceiver to the device controller in the functional circuits outside the integrated circuit includes passing analog USB signals from the transceiver to the device controller when the device controller includes a transceiver and passing transceived digital USB signals from the

transceiver to the device controller when the device controller does not include a transceiver [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

19. Referring to claim 8, Leydier teaches a method according to claim 6, wherein the interface integrated circuit does not include a USB device controller [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

20. Referring to claim 9, Leydier teaches an interface integrated circuit device according to claim 1, wherein the interface integrated circuit does not include a USB device controller [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

21. Referring to claim 10, Leydier teaches an interface integrated circuit device according to claim 1, wherein the interface integrated circuit is arranged to use USB communication from said host controller via the USB connection in a first speed mode when operating as a USB host and to use USB communication via the USB connection in a second speed mode, different from said first speed mode, as determined by the device controller when operating as a USB device [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

22. Referring to claim 11, Leydier teaches an electronic apparatus according to claim 3, wherein the device interface includes both an analog USB device interface and a transceived digital USB device interface for connection to the USB device controller circuit without and with an external transceiver, respectively [figures 3, 4, 5 and paragraphs 52-58 and 63-69.]

23. Referring to claim 12, Leydier teaches an electronic apparatus according to claim 3, wherein the interface integrated circuit does not include a USB device controller [figures 3, 4, 5 and paragraphs 52-58 and 63-69].

24. Referring to claim 13, Leydier teaches an electronic system according to claim 5, wherein the device interface includes both an analog USB device interface and a transceived digital USB device interface for connection to the USB device controller circuit without and with an external transceiver, respectively [figures 3, 4, 5 and paragraphs 52-58 and 63-69].

25. Referring to claim 14, Leydier teaches an electronic system according to claim 5, wherein the interface integrated circuit does not include a USB device controller [figures 3, 4, 5 and paragraphs 52-58 and 63-69].

26. Referring to claim 15, Leydier teaches an electronic system according to claim 5, wherein the system is arranged to use USB communication from said host controller via the USB connection in a first speed mode when operating as a USB host and to use USB communication via the USB connection in a second speed mode, different from said first speed mode, as determined by the device controller when operating as a USB device [figures 3, 4, 5 and paragraphs 52-58 and 63-69].

Conclusion

27. The examiner requests, in response to this Office Action, support be shown for language added to any original claims and any new claims presented by an amendment. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Furthermore, when responding to this Office Action, applicant is advised that if a traversal of an obviousness rejection under 35 U.S.C. 103 is presented, a reasoned statement must be included explaining why the applicant believes the Office has erred substantively as to the factual findings or the conclusion of obviousness See 37 CFR 1.111(b).

Additionally, applicant is further advised to clearly point out the patentable novelty which the applicant believes the claims preset, in view of the state of the prior art of record or the objections made. Applicant must also show how any new amendments overcome such references or objections, see 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NIKETA I. PATEL whose telephone number is (571)272-4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272 4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Niketa I. Patel/
Primary Examiner, Art Unit 2181